What is Claimed is:

1. During the testing of the operation of target processor by a host processing unit, a system for identifying the occurrence of a processor unit reset, the system comprising:

timing trace apparatus responsive to signals from the processor unit, the timing trace apparatus generating a timing trace stream;

program counter trace apparatus responsive to signals from the processing unit, the program counter trace apparatus generating a program counter trace stream; and

synchronization apparatus applying periodic signals to the timing trace apparatus and to the program counter trace apparatus, the periodic signals;

wherein the program counter trace apparatus is responsive to a reset signal, the program counter trace apparatus generating reset marker signal group identifying the occurrence of reset signal and relating the reset signal to the timing trace stream and the program execution.

2. The system as recited in claim 1 wherein the marker signal group includes a program counter address, a timing index and a periodic sync ID.

3. The system as recited in claim 1 further comprising:

data trace apparatus responsive to signals from the processing unit, the data trace apparatus generating a data trace stream, wherein the periodic sync ID signals are applied to the data trace apparatus provide periodic sync markers in the data trace stream; and

wherein the host processing unit is responsive to the timing trace stream, the program counter trace stream and the data trace stream, the host processing unit reconstructing the processing activity of the processing unit from the trace streams.

4. The system as recited in claim 1 wherein the program counter trace apparatus is responsive to the removal of the reset signal, the program counter trace apparatus generating a reset-off marker signal group, the reset-off marker signal group relating the occurrence of the reset signal to the timing trace stream and the program execution.

5. The method for communicating an occurrence of a reset signal from a target processor unit to a host processing unit, the method comprising:

generating a timing trace stream, a program counter trace stream, and data trace stream, and

in the program counter trace stream, including a marker signal group indicating an occurrence of reset signal and relating the occurrence to the data trace stream, to the timing trace stream, and to the program execution.

6. The method as recited in claim 5 further including:

in the marker signal group, including a periodic sync ID, a timing index and a program counter address.

7. The method as recited in claim 5 further comprising, when the reset signal is removed, including in the program counter trace stream a marker signal group indicating the occurrence of the removal of the signal group and relating the marker signal group to the timing trace stream and program execution.

8. In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, a marker signal group included in a trace signal stream, the marker signal group comprising:

indicia of the occurrence of a reset signal;

indicia of the relationship of the occurrence of the reset signal to the target processor clock; and

indicia of the relationship of the occurrence of the reset signal to the target processor program execution.

9. In a processing unit test environment wherein a target processor transmits a plurality of trace streams to a host processing unit, a marker signal group included in a trace signal stream, the marker signal group comprising:

indicia of the removal of a reset signal;

indicia of the relationship of the removal of the reset signal to the target processor clock; and

indicia of the relationship of the removal the reset signal to the target processor program execution.

10. In a target processing unit generating trace test signals for transfer to a host processing unit, program counter trace generation apparatus comprising:

a storage unit;

a decoder unit responsive to a rest signal for storing a signal group identifying the reset signal in the storage unit in a first location in the storage unit, the decoder unit generating a control signal;

a gate unit responsive to the control signal, the gate unit transmitting processor signals applied thereto to the storage unit for storage at defined locations, the signals stored in the storage unit forming a reset sync marker; and

a FIFO unit coupled to the storage unit, the FIFO unit receiving the reset sync marker when the reset signal marker is complete, the FIFO unit transferring the reset sync marker to the host processing unit.

11. The program counter trace apparatus as recited in claim 10 wherein the signals applied to the gate unit include a program counter address, a periodic sync ID, and a timing index.

12. The program counter trace apparatus as recited in claim 11 wherein when the reset signal is removed, a reset-off sync marker is generated in the storage unit.

13. The program counter trace apparatus as recited in claim 10 wherein the reset sync marker signal includes a plurality of packets.

14. The program counter trace apparatus as recited in claim 10 wherein the sync markers in the FIFO unit are transferred from the unit in response to control signals.